



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/631,185

07/31/2003

Gerard Chauvel

TI-35431

1444

23494

7590

03/16/2009

TEXAS INSTRUMENTS INCORPORATED

P O BOX 655474, M/S 3999

DALLAS, TX 75265

EXAMINER

SAVLA, ARPAN P

ART UNIT

PAPER NUMBER

2185

NOTIFICATION DATE

DELIVERY MODE

03/16/2009

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/631,185	<b>Applicant(s)</b> CHAUVEL ET AL.	
	<b>Examiner</b> Arpan P. Savla	<b>Art Unit</b> 2185	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 December 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### **Response to Amendment**

This Office action is in response to Applicant's communication filed December 22, 2008 in response to the Office action dated September 22, 2008. Claim 17 has been amended. Claims 1-20 are pending in this application.

## **REJECTIONS BASED ON PRIOR ART**

### **Claim Rejections - 35 USC § 102**

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 11 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Shen et al. (U.S. Patent 5,687,336) (hereinafter "Shen") with "The PC Guide: The Memory Controller" (hereinafter "PC Guide") offered as extrinsic evidence.**

3. **As per claim 11**, Shen discloses a computer system, comprising:  
a processor (col. 4, line 37; Fig. 2);

a memory coupled to the processor (col. 4, lines 33-34; Fig. 2, element 26); *It should be noted that the memory physically lies within the processor, thus making the memory and processor coupled.*

a stack that exists in memory and contains stack data (col. 4, lines 33-34; Fig. 2, element 26);

a memory controller coupled to the memory (col. 5, lines 19-23). *It should be noted that Shen does not expressly disclose a memory controller in the design, however, PC Guide states that every computer has within it a hardware logic circuit called the memory controller. Also, PC Guide states that the memory controller generates the necessary signals to control the reading and writing of information from and to the memory. Lastly, PC Guide states that the memory controller interfaces the memory with the other major parts of the computer system.*

trend logic (col. 4, lines 40-43; Fig. 2, element 20);

wherein the processor executes instructions (col. 4, lines 36-37);

wherein the trend logic provides trend information about the stack to the controller (col. 5, lines 10-14 and 19-22; Fig. 2, elements 20, 24, 40, and 94); *It should be noted that the trend information is calculated by the three-way addition of the stack pointer, segment base, and increment value (which comes from the increment logic) and then the trend information is sent from the three-port adder to the memory controller.*

wherein the trend information about the stack is based on at least one future instruction (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; Figs. 2 and 4).

4. **As per claim 13**, Shen discloses the trend logic determines a net stack trend based on current instruction and future instruction information coming from the decode logic (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15; col. 4, lines 36-60; Fig. 2, elements 20, 30, and 94).

5. **Claims 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Flake et al. (U.S. Patent 7,065,613) (hereinafter “Flake”).**

6. **As per claim 17**, Flake discloses a method, comprising:

issuing a write request to a cache memory, wherein the cache memory includes multiple cache lines (col. 5, line 55; col. 6, lines 4-5; Fig. 6);

determining whether the write request refers to a predetermined word within a dirty cache line (col. 5, lines 55-57; Fig. 5). *See the citation note for claim 6 below.*

determining whether to write the dirty cache line to main memory based on whether the size of a stack is increasing or decreasing (col. 6, lines 13-31).

7. **As per claim 18**, Flake discloses determining whether the write request will be to the end of a dirty cache line (col. 5, lines 55-57; Fig. 5). *See the citation note for claim 6 above.*

8. **As per claim 19**, Flake discloses the stack size is increasing and the dirty cache line is written to a main memory (col. 6, lines 13-28).

9. **As per claim 20**, Flake discloses the stack size is decreasing and the dirty cache line is retained in the cache memory (col. 6, lines 29-31).

**Claim Rejections - 35 USC § 103**

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. **Claims 1-4, 6-10, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen in view of Flake with PC Guide offered as extrinsic evidence.**

12. **As per claim 1**, Shen discloses a method of managing memory, comprising:

determining stack trend information using current and future stack operating instructions (col. 4, lines 11-15 and 36-60; Fig. 2; col. 3, line 65 – col. 4, line 7; col. 6, line 58 – col. 7, line 15; Fig. 4); *It should be noted that Shen's final value for the stack pointer indicates whether the stack size has increased or decreased.*

Shen does not disclose reducing data traffic between various levels of a memory based on the trend information.

Flake discloses reducing data traffic between various levels of a memory based on trend information (col. 6, lines 32-44). *It should be noted that the decision to skip reading the line from main memory is based on the stack operation.*

Shen and Flake are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Flake's miss algorithm to Shen's stack trend tracker system

because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of reducing the number of accesses to main memory.

13. **As per claim 2**, the combination of Shen/Flake discloses determining the trend information includes examining future instructions to determine if the size of the stack is going to decrease as a result of future instructions (Shen, col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-5 and 9-10; Figs. 2 and 4).

14. **As per claim 3**, the combination of Shen/Flake discloses a predetermined number of instructions are used in determining stack trend information (Shen, col. 3, lines 65-67; col. 6, lines 47-48). *It should be noted that if there is only one instruction per stage and there are five stages in the pipeline, then five instructions are used in determining stack trend information.*

15. **As per claim 4**, the combination of Shen/Flake discloses the number of predetermined instructions is at least two (Shen, col. 3, lines 65-67; col. 6, lines 47-48). *See citation note for claim 3 above.*

16. **As per claim 6**, the combination of Shen/Flake discloses determining which word of the dirty cache line is going to be written to (Flake, col. 5, lines 55-57; Fig. 5). *It should be noted that in Flake's cache each line contains 2 bytes (col. 5, line 48). Since 2 bytes = 1 word, it follows that in Flake's cache each line contains 1 word. Thus, once the algorithm chooses which dirty line to replace, as a consequence it has also determined which word of the dirty line (to be replaced) is going to be written to.*

17. **As per claim 8**, the combination of Shen/Flake discloses determining the trend information includes examining future instructions to determine if the size of the stack is going to increase as a result of future instructions (Shen, col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-7; Figs. 2 and 4).

18. **As per claim 7**, Shen discloses a method of managing memory, comprising:  
determining stack trend information using current and future stack operating instructions (col. 4, lines 11-15 and 36-60; Fig. 2; col. 3, line 65 – col. 4, line 7; col. 6, line 58 – col. 7, line 15; Fig. 4); *See the citation note for the same limitation in claim 1 above.*

utilizing the trend information to reduce data traffic between various levels of a memory (col. 8, lines 34-47). *It should be noted that the limitation “to reduce data traffic between various levels of a memory” is merely a recitation of intended use for the “trend information.” A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. It should also be noted that by having the stack pointer signal a mis-aligned access, push/pop pairing is prevented, a second cache access is prevented, thus, data traffic between various levels of the cache are reduced.*

Shen does not disclose the levels of memory comprise a cache memory containing multiple cache lines and a main memory, and wherein the trend information

is used to restrict writing dirty cache lines from cache memory to main memory when the trend information indicates the stack is decreasing.

Flake discloses the levels of memory comprise a cache memory containing multiple cache lines and a main memory (col. 6, lines 4-9; Fig. 6), and wherein the trend information is used to restrict writing dirty cache lines from cache memory to main memory when the trend information indicates the stack is decreasing (col. 6, lines 29-31). *It should be noted that a “deletion of a group of stack objects” is analogous to the “stack decreasing.”*

Shen and Flake are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Flake's miss algorithm to Shen's stack trend tracker system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of reducing the number of accesses to main memory.

19. **As per claim 9**, Shen discloses a method of managing memory, comprising:

determining stack trend information using current and future stack operating instructions (col. 4, lines 11-15 and 36-60; Fig. 2; col. 3, line 65 – col. 4, line 7; col. 6, line 58 – col. 7, line 15; Fig. 4), including determining if the size of the stack is going to increase as a result of future instructions (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-7; Figs. 2 and 4);

utilizing the trend information to reduce data traffic between various levels of a memory (col. 8, lines 34-47). *See the citation note for the same limitation in claim 7 above.*

Shen does not disclose determining if a line is written back including analyzing the trend information and including examining a dirty cache line to determine which word of the dirty cache line is going to be written to.

Flake discloses determining if a line is written back including analyzing the trend information (col. 6, lines 13-28) and including examining a dirty cache line to determine which word of the dirty cache line is going to be written to (col. 5, lines 55-57; Fig. 5). *See the citation note for claim 6 above.*

Shen and Flake are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Flake's miss algorithm to Shen's stack trend tracker system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of reducing the number of accesses to main memory.

20. **As per claim 10**, the combination of Shen/Flake discloses the dirty cache line is written from a cache memory to a main memory (Flake, col. 6, lines 22-23).

21. **As per claim 15**, Shen discloses a computer system, comprising:  
a processor (col. 4, line 37; Fig. 2);

a memory coupled to the processor (col. 4, lines 33-34; Fig. 2, element 26); *See the citation note for the same limitation in claim 11 above.*

a stack that exists in memory and contains stack data (col. 4, lines 33-34; Fig. 2, element 26);

a memory controller coupled to the memory (col. 5, lines 19-23). *It should be noted that Shen does not expressly disclose a memory controller in the design, however, PC Guide states that every computer has within it a hardware logic circuit called the memory controller. Also, PC Guide states that the memory controller generates the necessary signals to control the reading and writing of information from and to the memory. Lastly, PC Guide states that the memory controller interfaces the memory with the other major parts of the computer system.*

trend logic (col. 4, lines 40-43; Fig. 2, element 20);

wherein the processor executes instructions (col. 4, lines 36-37);

wherein the trend logic provides trend information about the stack to the controller (col. 5, lines 10-14 and 19-22; Fig. 2, elements 20, 24, 40, and 94); *See the citation note for the same limitation in claim 11 above.*

wherein the trend information about the stack is based on at least one future instruction (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; Figs. 2 and 4).

Shen does not disclose the memory includes a cache memory containing multiple cache lines and a main memory, and wherein the trend information is used to restrict writing dirty cache lines from cache memory to main memory when the trend information indicates the stack is decreasing.

Flake discloses the memory includes a cache memory containing multiple cache lines and a main memory (col. 6, lines 4-9; Fig. 6), and wherein the trend information is used to restrict writing dirty cache lines from cache memory to main memory when the trend information indicates the stack is decreasing (col. 6, lines 29-31). *See the citation note for the similar limitation in claim 7 above.*

Shen and Flake are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Flake's miss algorithm to Shen's stack trend tracker system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of reducing the number of accesses to main memory.

22. **As per claim 16**, Shen discloses a computer system, comprising:

a processor (col. 4, line 37; Fig. 2);

a memory coupled to the processor (col. 4, lines 33-34; Fig. 2, element 26); *See the citation note for the same limitation in claim 11 above.*

a stack that exists in memory and contains stack data (col. 4, lines 33-34; Fig. 2, element 26);

a memory controller coupled to the memory (col. 5, lines 19-23). *It should be noted that Shen does not expressly disclose a memory controller in the design, however, PC Guide states that every computer has within it a hardware logic circuit*

*called the memory controller. Also, PC Guide states that the memory controller generates the necessary signals to control the reading and writing of information from and to the memory. Lastly, PC Guide states that the memory controller interfaces the memory with the other major parts of the computer system.*

trend logic (col. 4, lines 40-43; Fig. 2, element 20);

wherein the processor executes instructions (col. 4, lines 36-37);

wherein the trend logic provides trend information about the stack to the controller (col. 5, lines 10-14 and 19-22; Fig. 2, elements 20, 24, 40, and 94); *See the citation note for the same limitation in claim 11 above.*

wherein the trend information about the stack is based on at least one future instruction (col. 3, line 65 – col. 4, line 7; col. 4, lines 11-15 and 36-60; Figs. 2 and 4).

Shen does not disclose the memory includes a cache memory and a main memory, and wherein the cache memory contains a dirty cache line, and wherein the dirty cache line is written to main memory if the trend information indicates the stack is increasing.

Flake discloses the memory includes a cache memory and a main memory (col. 6, lines 4-9; Fig. 6), and wherein the cache memory contains a dirty cache line (col. 6, lines 19-20), and wherein the dirty cache line is written to main memory if the trend information indicates the stack is increasing (col. 6, lines 13-28). *It should be noted that "stack growth" is analogous to the "stack increasing."*

Shen and Flake are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Flake's miss algorithm to Shen's stack trend tracker system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of reducing the number of accesses to main memory.

**23. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen in view of O'Connor et al. (U.S. Patent 6,026,485) (hereinafter "O'Connor").**

24. **As per claim 12**, Shen discloses all the limitations of claim 12 except an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions.

O'Connor discloses an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions (col. 3, lines 5-10, 15-18, and 42-48). *It should be noted that first instructions are current instructions while second instructions are future instructions.*

Shen and O'Connor are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply O'Connor's instruction decoder to Shen's stack trend tracker system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no

change in their respective functions, and the combination would have yielded the predictable results of instruction folding for a stack based machine.

25. **As per claim 14**, the combination of Shen/O'Connor discloses the second portion of the decoder is adjusted so that the number of future instructions that are decoded equals at least two (O'Connor, col. 3, lines 59-60). *It should be noted that first instructions are current instructions while second and third instructions are both future instructions.*

26. **Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shen in view of Flake as applied to claim 1, and further in view of Ebrahim et al. (U.S. Patent 5,893,121) (hereinafter "Ebrahim").**

27. **As per claim 5**, the combination of Shen/Flake discloses all the limitations of claim 5 except the cache memory maintains a single dirty cache line for stack data.

Ebrahim discloses the cache memory maintains a single dirty cache line for stack data (col. 5, lines 32-35). *It should be noted that a cache block maintaining a dirty bit is analogous to a "dirty cache line".*

The combination of Shen/Flake and Ebrahim are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Ebrahim's stack cache memory containing a single dirty cache line to Shen/Flake's stack trend tracker system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the

combination would have yielded the predictable results of automatically recovering memory objects no longer in use by the operating system and application programs in a computer system.

### **Response to Arguments**

28. Applicant's arguments filed December 22, 2009 with respect to **claims 1-16** have been fully considered but they are not persuasive.

29. With respect to Applicant's arguments regarding claims 1-16, which appear on pages 7-8 of the communication filed December 22, 2008, the Examiner respectfully disagrees.

Firstly, in response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the features upon which applicant relies (i.e., "reducing data traffic between various levels of a memory based on the trend information") are not recited in the rejected claims 7, 9, 11, 15, and 16. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Secondly, as discussed in the last Office action dated September 22, 2008, as commonly defined, a "trend" is "the general movement over time of a statistically detectable change." In Shen, a new stack pointer indicates the final value of the stack and therefore the new stack pointer reflects the general movement of the stack size over a period of time (the period of time being the time between the generation of the

old stack pointer and the generation of the new stack pointer). The various stages in Shen's pipelined processor contain both current and future instructions. These instructions are used to generate a new stack pointer. As detailed above, the new stack pointer reflects the "trend" of the stack and is therefore equivalent to "trend information." Accordingly, Shen sufficiently discloses determining stack trend information using future stack operating instructions, as simply and broadly claimed by Applicant.

Lastly, regarding claim 1 in particular, in Flake, the reduction of data traffic between various levels of a memory (i.e. the decision to skip reading a line from main memory) is based on the stack operation. Stack operations are the basis of the so called "trend information" as discussed directly above. Thus, it follows that in Flake the reduction of data traffic between various levels of a memory is based on "trend information", as simply and broadly claimed by Applicant.

30. Applicant's arguments filed December 22, 2009 with respect **to claims 17-20** have been considered but are moot in view of the new ground of rejection above.

31. As for Applicant's arguments with respect to the dependent claims, the arguments rely on the allegation that the independent claims are allowable and therefore for the same reasons the dependent claims are allowable. However, as addressed above, the independent claims are not allowable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

### **Conclusion**

### **STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

**CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, **claims 1-20** have received an action on the merits and are subject of a final action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/  
Examiner, Art Unit 2185  
March 8, 2009

/Sanjiv Shah/  
Supervisory Patent Examiner, Art  
Unit 2185